CURRICULUM AND SYLLABUS OF M.TECH DEGREE PROGRAMME IN MICROELECTRONICS AND VLSI DESIGN

(Effective from 2017 Admitted Batch onwards)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY, SIKKIM

Curriculum for M. Tech. in Microelectronics and VLSI Design

Semester I

S. No.	Code	Name of the Subject	L	T	P/S	C
1.	EC21101	Introduction to VLSI Design	3	0	0	3
2.	EC21102	Semiconductor Device Theory and Modelling	3	0	0	3
3.	EC21103	VLSI Technology and Processing	3	0	0	3
4.	EC21104	Analog Integrated Circuit Design	3	0	0	3
5.	EC21105	Modelling of Digital System	3	0	0	3
6.	EC21201	Semiconductor device simulation and process modeling Lab	0	0	4	2
7.	EC21202	Modelling of digital system Lab	0	0	4	2
		Total credits				19

Semester II

S. No.	Code	Name of the Subject	L	T	P/S	C
1.	EC22101	MOS Device Modelling	3	0	0	3
2.	EC22102	VLSI System Design	3	0	0	3
3.		Elective I	3	0	0	3
4.		Elective II	3	0	0	3
6.	EC22103	Semiconductor Materials and Device characterization	3	0	0	3
7.	EC22201	VLSI Design Lab	0	0	4	2
8.	EC22201	Mini Project on SOC	0	0	2	2
9.	EC22242	Viva Voice	-	-	-	1
9.	EC 22242	Student summer internship (Will be evaluated in 3rd semester)	-	-	-	-
		Total credits				20

Semester III

S. No.	Code	Name of the Subject	L	T	P/S	C
1.		Project Work Phase I				
	EC23401	Seminar and Viva Voce	-	-	-	10

	EC23402	Dissertation and thesis	-	-	-	10
2.	EC22242	Evaluation of internship (2nd Semester)	-	-	-	1
		Total credits				21

Semester IV

S. No.	Code	Name of the Subject	L	T	P/S	C
1.		Project Work Phase II				
	EC24401	Final Seminar and Viva Voce	-	-	-	10
	EC24402	Dissertation and thesis	-	-	-	10
		Total credits				20

Minimum Requirements

Minimum number of credits to be earned by a student is 80

List of Electives

S.No.	Code	Name of the Subject	L	T	P/S	C
1.	EC21301/ EC22301	Compound Semiconductors: Properties & Applications	3	0	0	3
2.	EC21302/ EC22302	MEMS and Microsystems	3	0	0	3
3.	EC21303/ EC22303	Foundation of VLSI CAD	3	0	0	3
4.	EC21304/ EC22304	Testing & Verification of VLSI Circuits	3	0	0	3
5.	EC21305/ EC22305	Semiconductor Power Devices	3	0	0	3
6.	EC21306/ EC22306	Nanoelectronics	3	0	0	3
7.	EC21307/ EC22307	Low Power CMOS VLSI design	3	0	0	3
8.	EC21308/ EC22308	Mixed Signal RF ICdesign	3	0	0	3
9.	EC21309/ EC22309	CMOS RF circuit design	3	0	0	3
9.	EC21310/ EC22310	III-V semiconductors and High Speed electronic Devices	3	0	0	3
11	EC21311/ EC22311	VLSI for Signal Processing	3	0	0	3

*Any one elective may be offered as global elective for specific departments.

*Any other subject (core/elective) offered by the Department from time to time shall be taken as elective with the consent of course co-ordinator/faculty.

Syllabus of M. Tech. Degree Programme in Microelectronics and VLSI Design

SEMESTER-I

EC21101: Introduction to VLSI Design

L	T	P/S	C
3	0	0	3

Module 1 (11 hours)

Introduction MOSFET, threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitics, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Module 2 (10 hours)

CMOS inverter, static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

Module 3 (13 hours)

Static CMOS design, Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS –Course project

Module 4 (8 hours)

Circuit design considerations of Arithmetic circuits, shifter, CMOS memory design - SRAM and DRAM, BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, , MGH, Third Ed., 2003

2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective,Prentice Hall, Second Edition, 2005

3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, Third Edition, McGraw-Hill, 2004

4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation, Wiley-IEEE Press, 2007

5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill

Professional, 2001

EC21102: Semiconductor Device Theory and Modelling

L	T	P/S	C
3	0	0	3

Module 1 (16 hours)

Review of quantum mechanics, Electrons in potentials (infinite barrier, potential well), Electrons in periodic lattices (KP Model), E-k diagrams, effective mass; Quasi-particles in semiconductors, electrons, holes (light holes and heavy holes), optical and acoustic phonons, electron hole pair (EHP). Band diagram of silicon, intrinsic and extrinsic carrier concentration, relation between applied voltage and Fermi level, Carrier statistics; Generation-recombination, SRH theory, diffusion length, carrier life time, Continuity equation, Poisson's equation and solution, Boltzmann transport equation, Mobility and diffusivity; variation of mobility with temperature, doping, high filed mobility, low field mobility, Hall mobility/Hall experiment, sheet resistance, drift and diffusion.

Module 2 (14 hours)

Junction devices- PN junction diode: band diagrams, electrostatics of a pn junction diode, CV characteristics, IV characteristics, high level injection, low level injection, ac characteristics: admittance of a diode, break down phenomenon in diodes; MS contact, band diagrams, ohmic and non ohmic contacts, thermionic Emission model for current transport and current-voltage (I-V) characteristics, effect of interface states and interfacial thin electric layer on the Schottky barrier height and the I-V characteristics; Solar cells

Module 3 (12 hours)

Bipolar Junction Transistors (12 hours): Structure of a BJT, carrier statistics in base, emitter, collector, figures of merit, basic principle of operation, long base transistor, short base transistor, analysis of ideal diffusion transistor, Ebers-Moll model, narrow base effects, narrow emitter effects, current crowding, effect of narrow base width and emitter width on device figures of merit, high level injection effects, Kirk effect, BJT at high frequencies

References:

1. M.S.Tyagi, John, Introduction to Semiconductor materials and Devices, Wiley & Sons, ISBN: 9971-51-316-1

2. Donald A Neamen, Semiconductor Physics and Devices: Basic Principles, McGraw-Hill (1997) ISBN 0-256-24214-3

3. Ben G. Streetman (2000), Solid State Electronic Devices, 5th Edition, ISBN 0-13-0257060

4. S.M. Sze, Modern Semiconductor Device Physics, Wiley (1998) ISBN 0-471-15237-4

5. J.P.Colinge, C.A.Colinge, Physics of Semiconductor Devices, Kulwer Academic Publishers, ISBN 1-40207-018-7 (available online at NITC intranet, in Springer eBook library, status 15th March 2010)

6. Yuan Taur & Tak H Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998.

7. S M Sze, High speed semiconductor devices, John Wiley, 1990

8. Donald A Neamen and Dhrubes Biswas“ Semiconductor Physics and Devices: Basic Principles, McGraw-Hill”

EC21103: VLSI Technology and Processing

L	T	P/S	C
3	0	0	3

Module 1 (6 hours)

Material properties, crystal structure, lattice, basis, planes, directions, angle between different planes, defects, characterization of material based on band diagram and bonding, conductivity, resistivity, sheet resistance, phase diagram and solid solubility, Crystal growth techniques, Heterostructures, wafer cleaning, Epitaxy, Clean room and safety requirements

Module 2 (15 hours)

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films, Deal-Grove model and Improvements in Deal-Grove method for thin and ultra thin oxide layers, thickness characterization methods, multi dimension oxidation modeling

Diffusion and Ion Implantation: Diffusion process, Solid state diffusion modeling, various doping techniques, Ion implantation, modeling of Ion implantation, statistics of ion implantation, damage annealing, thermal budget, rapid thermal annealing, spike anneal, advanced annealing methods, Implant characterization SIMS, spreading resistance method

Module 3 (15 hours)

Deposition & Growth**:** Homogeneous and Heterogeneous growth**,**Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating, LPCVD, epitaxy, MBE, ALCVD, Growth of High k and low k dielectrics

Etch and Cleaning**:** materials used in cleaning, various cleaning methods, Wet etch, Dry etch, Plasma etching, RIE etching, etch selectivity/selective etch

Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, Resolution, Depth of Focus, Numerical Aperture (NA), sensitivity, contrast, need for different light sources, masks, Contact, proximity and projection lithography, step and scan, optical proximity correction, develop(development of resist), Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL

Module 4 (6 hours)

Planarization Techniques: Need for planarization, Chemical Mechanical Polishing. Metallization and Interconnects: Copper damascene process, Metal interconnects; Multi-level metallization schemes, Process integration: NMOS, CMOS and Bipolar process.

Reference:

1. M. Deal and P.Griffin, Silicon VLSI Technology, James Plummer, Prentice Hall Electronics, 2010.

2. Stephen Campbell, The Science and Engineering of Microelectronics Oxford University Press, 1996. 3. S.M. Sze, VLSI Technology, 2nd Edition, McGraw Hill, 1988. 4. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983. 5. C.Y. Chang and S.M.Sze , ULSI Technology, McGraw Hill Companies Inc, 1996.

3. Ayers J. E Heteroepitaxy of Semiconductors Theory, Growth, and Characterization (CRC Press, Taylor & Francis Group, New York, 2007)

4. S. M.Sze, " VLSI Technology" McGraw-Hill, 1983.

5. S. K. Gandhi, "VLSI fabrication principles", 1983.

EC21104: Analog Integrated Circuit Design

L	T	P/S	C
3	0	0	3

Module I (10 Hrs):

Introduction to Analog Design, Basic MOS Device Physics: MOSFET as a switch, MOS I/V characteristics and MOS Device model.

Module II (10 hrs)

Amplifiers: Analysis of Single stage and Differential amplifiers. Passive and Active Mirrors, Frequency Response of Amplifiers, Noise: Statistical Characteristic of Noise, Type of Noise, and Noise in Single stage amplifiers.

Module III (10 hrs)

Feedback topologies, Effect of Loading, Operational Amplifiers, Stability and Frequency Compensation, Bandgap References, Introduction to switched Capacitor Circuits, Nonlinearity and Mismatch, Osillators,

Module IV (10)

Short-channel Effects and Device Models: Scaling theory, Threshold Voltage Variation, Mobility Degradation with Vertical field, Velocity Saturation, Hot Carrier effect, MOS device Models: Level 1 model, level 2 model, level 3 model, charge and Capacitance Modeling, Temperature dependence.

References:

1. David A Johns & Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 2002.
3. Philip Allen & Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002.

EC21105: Modelling of Digital System

L	T	P/S	C
3	0	0	3

Module 1(8 hours): Programming Technologies – ROMs & EPROMs PLA . PAL gate Arrays Programmable gate arrays and applications, Antifuse FPGA, Synthesis methods for FPGA.

Module 2(8 hours): Hardware Description Language. Design entities, architecture Bodies, Block Statements, processes data types. Operators . Classes of Objects, Attributes, Functions and Procedures, Packages Control Statements.

Module 3(8 hours): Behavioral modeling.- Process Statement, Assertion Statement, Sequential wait Statement, Formatted ASCII I/O Operations Structural Modeling ; parts Library wiring of Primitives. Wiring of Iterative networks. Modeling a test bench.

Module 4(10 hours): Chip Level Modeling : Chip level modeling structures modeling delay, process model graphs, Functionally partitioned models, Timing Assertion, Setup & Hold time for clocked devices, Design rule checks System Modeling : Modeling system interconnection, general model for signal interconnection, Multiplexing of signals. Multiple valued logic. Processor model. RAM model. UART model, Parallel I/O Ports, Interrupt controller Simulation with the physical model, simulation, writing test bench, converting real and interconnection, Multiplexing of signals. Multiple valued logic. Processor model. RAM model. UART model, Parallel I/O Ports, Interrupt controller.

Module 5(8 hours): Simulation with the physical model, simulation, writing test bench, converting real and integer to time. Dumping results into text file, reading vectors from text file, test bench example.

Reference:

1. Navabi Z, “VHDL Analysis and Modeling of Digital Systems”. Prentice Hall, 1993.
2. J. Bhasker “VHDL Primer”, Pearson Education, 2000.
3. Armstrong & Grey. “VHDL Design. Representation and Synthesis”, PHPTR, 2000.
4. James R. Armstrong, “Chip Level Modeling with VHDL”, Prentice hall, 1989.

EC21201: Semiconductor device simulation and process modelling lab

L	T	P/S	C
0	0	4	2

Familiarization of Simulator:

Know how of gridding techniques (adaptive gridding), various modules in the simulator (process module (2D & 3D), device module (2D & 3D), mixed mode module etc.), information on models. In doing so a simple experiment as described below may be planned.

PN diode simulations:

2D simulations (4 sessions): Use device simulator to generate a pn diode structure. Simulate I-V characteristics and also get the C-V characteristics. Find the carrier concentration, electron and hole concentration, electric field, potential distribution (at different biases) and doping distribution across the structure. Check the current and capacitance values with hand calculations. Extract V_{bi} from capacitance characteristics. Freeze different models one used. Process simulate the same structure with same/similar doping levels. Exporting the process simulated structure in to device simulator, extract I-V and C-V characteristics and make similar observations as in device simulation and explain the differences if any.

3D simulations (2 sessions): The effect of series resistance is very important and most of the times a series resistance is what determines the current through pn diode. This experiment aims to simulate such an effect (no need a mixed mode simulator). Study the effect of series the on current through the device with change in series resistance.

BJT simulations:

2D simulations (3 sessions): Bipolar devices are very important devices to understand. Any given MOSFET has a parasitic BJT. If not taken care in device design, the parasitic BJT may lead to very different behavior. The aim of these experiments is to understand the different effects in BJT. For a lateral/planar BJT, the following experiments can be performed:

1) Variation in and with base doping and base width and respective current dc characteristics
2) Variation, and with emitter width and respective current characteristics

3D simulations (2 sessions): For a Vertical BJT effect of poly emitter on device performance, carrier concentration, electron and hole concentration, potential and electric field distributions across the BJT, impact ionization.

References:

1. User manuals of software used in the labs.
2. Donald A Neamen, Semiconductor Physics and Devices: Basic Principles, McGraw-Hill (1997) ISBN 0-256-24214-3.
3. Ben G. Streetman, Solid State Electronic Devices, 5th Edition, (2000), ISBN 0-13-025706-0.
4. S.M. Sze, Modern Semiconductor Device Physics, Wiley (1998) ISBN 0-471-15237-4.
5.Robert F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley (1995), ISBN 020154393-1, (Indian edition available).
6. M.S.Tyagi, Introduction to Semiconductor materials and Devices, John Wiley & Sons, ISBN: 9971-51-316-1.

EC21202: Modelling of Digital system Lab

L	T	P/S	C
0	0	4	2

1. Write VHDL programs for the following circuits, check the wave forms.
   a. Half adder b. Full adder
2. Design and simulation of 4-bit adder using VHDL
3. Write VHDL programs for the following circuits, check the wave forms.
   a. Multiplexer b. Demultiplexer
4. Write VHDL program for encoder and check the wave forms.
5. Write a VHDL program for a decoder and check the wave forms.
6. Write a VHDL program for a Down counter and check the wave forms.
7. Write a VHDL program for a T FLIP-FLOP and check the wave forms.
8. Design and simulation of sequential circuit using VHDL.
9. Design and simulation of FSM circuit using VHDL
10. Design and simulation of counter using VHDL
11. Implement Half Adder using FPGA & CPLD.
12. Implement Full Adder using FPGA & CPLD.
13. Implement Delay Flip flop using FPGA & CPLD.
14. Implement BCD to 7 segments Decoder using FPGA& CPLD.
15. Implement an Up Counter using FPGA & CPLD.

List of Equipments/Machine Required:
PCs with PIV/4GB RAM/40 GB HD, VHDL, Any Device Simulator

SEMESTER-II

EC22101: MOS Device Modelling

L	T	P/S	C
3	0	0	3

Module 1 (13 hours)

Semiconductor surfaces, Ideal MOS structure, MOS device in thermal equilibrium, Non-Ideal MOS: work function differences, charges in oxide, interface states, band diagram of non ideal MOS, flatband voltage, electrostatics of a MOS (charge based calculations), calculating various charges across the MOSC, threshold voltage, MOS as a capacitor (2 terminal device), Three terminal MOS, effect on threshold voltage.

Module 2 (10 hours)

MOSFET (Enhancement and Depletion MOSFETs), mobility, on current characteristics, off current characteristics, sub threhsold swing, effect of interface states on sub threshold swing, drain conductance and transconductance, effect of source bias and body bias on threshold voltage and device operation.

Module 3 (6 hours)

Scaling, Short channel and narrow channel effects- High field effects.

Module 4 (5 hours)

MOS transistor in dynamic operation, Large signal Modeling, small signal model for low, medium and high frequencies.

Module 5 (8 hours)

SOI concept, PD SOI, FD SOI and their characteristics, threshold voltage of a SOI MOSFET, Multi-gate SOI MOSFETs, Alternate MOS structures.

References:

1. E.H. Nicollian, J. R. Brews, Metal Oxide Semiconductor - Physics and Technology, John Wiley and Sons.

2. Nandita Das Guptha, Amitava Das Guptha, Semiconductor Devices Modeling and Technology, Prentice Hall India

3. Jean- Pierrie Colinge, Silicon-on-insulator Technology: Materials to VLSI, Kluwer Academic publishers group.

4. Yannis Tsividis, Operation and Modeling of the MOS transistor, Oxford University Press.

5. M.S.Tyagi, Introduction to Semiconductor materials and Devices, John Wiley & Sons, ISBN: 9971-51-316-1.

EC22102: VLSI System Design

L	T	P/S	C
3	0	0	3

Module 1 (11 hrs)

Introduction to digital IC design –Custom and semicustom flow, combinational logic synthesis – Technology independent and technology dependent optimization –Logic synthesis -High level synthesis- Scheduling and allocation-ASAP and ALAP scheduling-Register allocation-Functional unit allocation-Interconnect path allocation-Hardware description languages-synthesis-register transfer design-Event driven simulation.

Module 2 (11 hrs)

Subsystem design principles-pipelining-Data paths in processor architecture –Standard cell layout-Logic design considerations of adder and multiplier- Timing -Slack delay model – Effect of skew and jitter on timing, Sources of skew and jitter- Clocking disciplines -Wire model-Technology scaling effect on interconnect and -Noise in interconnects.

Module 3 (11 hrs)

Partitioning-Floorplanning and pin assignment-Slicing tree –Channel definition-Channel routing order-Wind mill constraint-Placement-Special routing-Clock routing for regular and irregular structures-Power routing-Global routing-Line Probe algorithm-Maze routing-Detail routing-Left edge algorithm-Vertical constraint-switch box routing.

Module 4 (9 hrs)

FPGA logic element and interconnect architecture-logic synthesis for FPGA-Physical design for FPGA-I/O circuits, ESD protection, Off chip connections.

References:

1. James R.Armstrong, F.Gail Gray, VHDL Design Representation and Synthesis, Pearson education, 2007.

2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.

3. Wayne Wolf, FPGA-Based System Design, Pearson, 2009.

4. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer,Third edition,1999.

EC22103: Semiconductor Materials and Device Characterization

L	T	P/S	C
3	0	0	3

Module I (10 hrs): Structural Characterizations

High Resolution X-Ray Diffraction stydy (HRXRD), Field Emission Scanning Electron Microscopy analysis (FESEM), High resolution transmission Electron Microscopy analysis(HRTEM), Scanning Probe Microscopic Analysis (SPM)

Module II (7 hrs): Optical Characterizations

Ellipsometry, Photoluminescence, UV-Visible spectroscopy, FTIR, Raman spectroscopy, X-Ray Photolectron spectroscopy analysis (XPS)

Module III (15 hrs): Electrical Characterization

Resistivity (r): Four point probe, Spreading Resistance, Microwave and RF absorption methods.

Carrier density (n, p): Hall Effect, I-V, C-V, Capacitance-Voltage (C-V), Optical absorption,

Carrier mobility (m): Resistivity and Hall Effect, Magnetoresistance

Module IV (8hrs): Chemical and Physical Characterization, Auger Electron Spectroscopy(AES), Secondary Ion Mass Spectroscopy(SIMS), Rutherford Back Scattering(RBS).

Reference:

1. Dieter K. Schroder, “Semiconductor Material and Device Characterization” John Wiley & Sons, INC, Second Edition.

2. Ayers J. E “Heteroepitaxy of Semiconductors Theory, Growth, and Characterization” (CRC Press, Taylor & Francis Group, New York, 2007),

3. D. Keith Bowen and Brain K. Tanner, “High Resolution X-ray Diffractometry and Topography” Tailor & Francis.

EC22201: VLSI Design Lab

L	T	P/S	C
0	0	4	2

1. Synthesis with timing constraints
2. Clock tree synthesis
3. Low power synthesis
4. Pre layout simulation
5. Floorplanning
6. Placement
7. Routing
8. Parasitic extraction
9. Post layout simulation
10. Standard cell layout

References:

1. James R.Armstrong, F.Gail Gray, VHDL Design Representation and Synthesis, Pearson education, 2007.

2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.

3. Wayne Wolf, FPGA-Based System Design, Pearson, 2009.

4. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer, Third edition,1999.

EC22202: Mini Project on SOC

L	T	P/S	C
0	0	2	2

EC22241: Viva Voice

L	T	P/S	C
0	0	0	1

EC22242: Student summer internship (To be evaluated in 3rd Semester)

SEMESTER-III

EC23401: Project Work Phase I

(a) Seminar and Viva Voce

L	T	P/S	C
-	-	-	10

(b) Dissertation and Thesis

L	T	P/S	C
-	-	-	10

(c) EC 22242: Evaluation of summer internship

L	T	P/S	C
-	-	-	1

SEMESTER-IV

EC24401: Project Work Phase II

(a) Seminar and Viva Voce

L	T	P/S	C
-	-	-	10

(b) Dissertation and thesis

L	T	P/S	C
-	-	-	10

LIST OF ELECTIVES

EC21301/EC22301: Compound Semiconductors: Properties & Applications

L	T	P/S	C
3	0	0	3

Module 1 (6 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature; important parameters governing the high power performance of devices and circuits: Break down voltage, resistances, device geometries, doping concentration and temperature.

Module 2 (16 hours)

Materials properties: Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices, outline of the crystal structure, dopants and electrical properties such as carrier mobility, velocity versus electric field characteristics of these materials, electric field characteristics of materials and device processing techniques, Band diagrams, homo and hetro junctions, electrostatic calculations, Band gap engineering, doping, Material and device process technique with these III-V and IV – IV semiconductors.

Module 3 (8 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Schottky barrier diode, Metal semiconductor Field Effect

Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

Module 4 (12 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices; High Frequency resonant –tunneling devices, Resonant-tunneling hot electron transistors

References:

1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications, Wiley & Sons.

2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons.

3. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams & Co., 1985

4. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.

5. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5

6. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,

7. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0-12-691740-X.

8. G.A. Armstrong, C.K. Maiti, TCAD for Si, SiGe and GaAs Integrated Circuits, The Institution of Engineering and Technology, London, United Kingdom, 2007,ISBN 978-0-86341-743-6.

9. Ruediger Quay, Gallium Nitride Electronics, Springer 2008, ISBN 978-3-540-71890-1, (Available on NITC intranet in Springer eBook section).

10. Prof. Dr. Alessandro Birolini, Reliability Engineering Theory and Practice, Springer 2007, ISBN-10 3-540-40287-X, Available on NITC intranet in Springer eBook section).

EC21302/EC22302: MEMS and Microsystems and NEMS

L	T	P/S	C
3	0	0	3

Module 1 (6 Hours)

An introduction to Micro sensors and MEMS, Evolution of Micro sensors & MEMS, Micro sensors & MEMS applications

Module 2 (12 Hours)

Microelectronic technologies for MEMS, Micromachining Technology, Surface and Bulk Micromachining, working principle of various MEMS.

Module 3 (12 Hours)

Micro machined Micro sensors: Mechanical, Inertial, Biological, Chemical, Acoustic, Microsystems Technology, Integrated Smart Sensors and MEMS.

Module 4 (12 hours)

Interface Electronics for MEMS, MEMS Simulators, MEMS for RF Applications, Bonding & Packaging of MEMS, Conclusions & Future Trends.

References:

1. Tai-ran Su, MEMS and Microsystems: design and Manufacture, Tata McGraw Hill.
2. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), VLSI Technology, McGraw Hill, 1988.
4. Julian W. Gardner, V. K. Varadan, Osama O. Awadelkarim, Microsensors, MEMS, and Smart Devices, ISBN: 047186109X - John Wiley and Sons.
5. Gere & Timoshenko, Mechanics of Materials, PWS-KENT, 1990.
6.Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WGB/McGraw-Hill,2000, ISBN: 0072907223.
7. M. Madou, Fundamentals of Microfabrication, CRC Press, 2002, ISBN: 0849308267
8. M. Elwenspoek & H. Jansen, Silicon micromachining, Cambridge, 1998, ISBN: 052159054
9. S. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001, ISBN: 0792372468
10. S.Sze, Semiconductor Sensors, John Wiley & Sons, 1994 ISBN: 0471546097
11. Marc Madou, Fundamentals of Microfabrication, CRC Press, 1997.

EC21303/EC22303: Foundations of VLSI CAD

L	T	P/S	C
3	0	0	3

Module 1 (10 hours)

Matrices: Linear dependence of vectors, solution of linear equations, bases of vector spaces, orthogonality, complementary orthogonal spaces and solution spaces of linear equations.

Module 2 (12 hours)

Graphs: representation of graphs using matrices; Paths, connectedness; circuits, cutsets, trees; Fundamental circuit and cutset matrices; Voltage and current spaces of a directed graph and their complementary orthogonality.

Module 3 (12 hours)

Algorithms data structures: efficient representation of graphs; Elementary graph algorithms involving bfs and dfs trees, such as finding connected and 2- connected components of a graph, the minimum spanning tree, shortest path between a pair of vertices in a graph

Module 4 (8 hours)

Data structures such as stacks, linked lists and queues, binary trees and heaps. Time and space complexity of algorithms

References:

1. K. Hoffman and R.E. Kunze, Linear Algebra, Prentice Hall (India), 1986
2.N.Balabanian and T.A. Bickart, Linear Network Theory: Analysis, Properties, Design and Synthesis, Matrix Publishers, Inc., 1981.
3. T.Cormen, C.Leiserson and R.A.Rivest, Algorithms, MIT Press and McGraw-Hill, 1990.
4. Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Second

Edition, Addison Wesley, 1993.
5. Neil H. E. Weste and David Harris, Principles of CMOS VLSI Design, Third Edition, Addison Wesley, 2004.

EC21304/EC22303: Testing and Verification of VLSI Circuits

L	T	P/S	C
3	0	0	3

Module 1 (10 hours)
Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SOCs.

Module 2 (14 hours)
Fundamentals of VLSI testing Fault models. Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan. System testing and test for SOCs. Delay fault testing.

Module 3 (9hours)
BIST for testing of logic and memories, Test automation, Design verification techniques based on simulation, analytical and formal approaches.

Module 4 (9hours)
Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

References:

1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers, 2000.
2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1990.
3. T.Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000.
4.P. Rashinkar, Paterson and L. Singh, System-on-a-Chip Verification-Methodology and Techniques, Kluwer Academic Publishers, 2001.
5. Neil H. E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Second Edition, Addison Wesley, 1993.
6. Neil H. E. Weste and David Harris, Principles of CMOS VLSI Design, Third Edition, Addison Wesley, 2004.

EC21305/EC22305: Semiconductor Power Devices

L	T	P/S	C
3	0	0	3

Module 1 (10 hours)

Avalanche Breakdown voltage of plane and planar pn junctions, Breakdown voltage improvement Techniques.

High injection level effects in pn junctions. Forward voltage drop in high voltage PIN diodes, and its dependence on carrier lifetime.

Module 2 (14 hours)

Bipolar Power Transistor structures and characteristics, Current-gain, Switching operation, second break down and safe operating area, overlay transistor.

Thyristor operation principles, Reverse and forward blocking voltage and forward conduction characteristics. Cathode shorted and Anode shorted Thyristor. di/dt and dv/dt ratings of thyristors, Triacs and GTO.

Module 3 (14 hours)

Power MOSFET structure, I-V characteristics, on resistance, Minimum size chip design for specific drain breakdown voltage, Switching characteristics, Safe operating area, Insulated Gate Transistor (IGT) –Structure, Operation principle, I-V characteristics and turn off transients, Latch up and its prevention.

Module 4 (6 hours)

Power Integrated Circuit Problems and isolati

References:

1. Baliga, B. Jayant, Power Semiconductor Devices, PWS Publishing Co., Boston, 1996

2. Benda, Vitezslav, John Gowar, and Duncan A. Grant, Chichester , Power semiconductor devices: theory and applications, New York Wiley, c 1999

3. Bose, Bimal K, Modern Power Electronics, Evolution, Technology, and Application, IEEE Press, 1992.

4. Ramshaw, Raymond S., Power Electronics Semiconductor Switches, 2nd ed., London: Chapman & Hall (Kluwer)

5.Rashid, Muhammad H., Upper Saddle River, Power Electronics, Circuits, Devices and Applications, 3rd ed., NJ: Pearson Education, 2003.

EC21306/EC22306: Nanoelectronics

L	T	P/S	C
3	0	0	3

Module 1 (8 hours)

Introduction of Nanoscience and Technology,Challenges going to sub-100 nm MOSFETs – Oxide layer thickness, tunnelling, power density, non-uniform dopant concentration, threshold voltage scaling, lithography, hot electron effects, sub-threshold current, velocity saturation, interconnect issues, fundamental limits for MOS operation. High-K gate dielectrics, effects of high-K gate dielectrics on MOSFET performance,

Module 2 (12 hours)

Novel MOS-based devices –Multiple gate MOSFETs, Silicon-on-nothing, Silicon-on-insulator devices, FD SOI, PD SOI, FinFETs, vertical MOSFETs, strained Si devices

Module 3 (6 hours)

Hetero structure based devices –Type I, II and III Heterojunction, Si-Ge heterostructure, hetero structures of III-V and II-VI compounds - resonant tunnelling devices, MODFET/HEMT

Module 4 (8 hours)

Carbon nanotubes based devices –CNFET, characteristics, Spin-based devices –spinFET, characteristics

Module 5 (8 hours)

Quantum structures –quantum wells, quantum wires and quantum dots, Single electron devices –charge quantization, energy quantization, Coulomb blockade, Coulomb staircase, Bloch oscillations

References:

1. Mircea Dragoman and Daniela Dragoman, Nanoelectronics –Principles & devices, Artech House Publishers, 2005.

2. Karl Goser, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2005.

3. Mark Lundstrom and Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2005.

4. Vladimir V Mitin, Viatcheslav A Kochelap and Michael A Stroscio, Quantum heterostructures, Cambridge University Press, 1999.

5. S.M. Sze (Ed), High speed semiconductor devices, Wiley, 1990.

6. Manijeh Razeghi, Technology of Quantum Devices, Springer, ISBN 978-1-4419-1055-4.

7. H.R. Huff and D.C. Gilmer, High Dielectric Constant Materials for VLSI MOSFET Applications, Springer 2005, ISBN 978-3-540-21081-8 , (Available on NITC intranet in Springer eBook section) 8.B.R. Nag, Physics of Quantum Well Devices, Springer 2002, ISBN 978-0-7923-6576-1, (Available on NITC intranet in Springer eBook section).

EC21307/EC22307: Low Power CMOS VLSI design

L	T	P/S	C
3	0	0	3

Module 1(12 hours)

Review of power dissipation in CMOS Circuits –static and dynamic power dissipation-Leakage sources, input vector dependence, stack effect, leakage reduction using natural and forced stacks, power gating, power gating methodologies, dynamic voltage scaling, forward and reverse body bias, standby techniques, MTCMOS circuits, level shifters, timing and power planning, choosing the high V_{TH} value, MTCMOS circuits using sleep transistors

Module 2 (14 hours)

Supply voltage scaling approaches: parallelism, pipelining, using multiple supply voltage, module level voltage selection, clustered voltage scaling, level converters, multiple supplies inside a block, supply voltage limitations, Optimum supply voltage, multiple device threshold, Technology level –feature size scaling, threshold voltage scaling, Transistor sizing for energy minimization, dynamic supply voltage scaling, dynamic threshold voltage scaling

Module 3 (6 hours)

Switching activity estimation in static and dynamic logic, signal statistics, intersignal correlations, Reducing switching capacitance through transistor sizing, logic and architecture optimization, layout techniques, logic restructuring, input ordering, data representation, resource allocation, reducing glitching through path balancing, clock gating

Module 4 (10 hours)

Behavioral level transforms, algorithm level transforms, architectural transformations, Operation reduction and substitution, logic level optimization and technology mapping,

Energy recovery, design with reversible logic, adiabatic logic, peripheral circuits, Power gating, signal isolation, state retention and restoration, architectural issues for power gating, Dynamic voltage and frequency scaling.

References:

1. Anantha Chandrakasan, Robert Brodersen, Low-power CMOS design, IEEE press, 1998
2. Kaushik Roy, Sharat C. Prasad, Low-power CMOS VLSI circuit design, John Wiley & Sons, 2000.
3. A.Bellamour, M.I.Elmasri, Low power VLSI CMOS circuit design, Kluwer Academic Press, 1995
4. Siva G.Narendran, Anantha Chandrakasan, Leakage in Nanometer CMOS Technologies, Springer, 2005.
5. Mohab Anis, Mohamed Elmasry, Multi-Threshold CMOS Digital Circuits, Kluwer Academic Publishers, 2003.
6. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, Low power methodology manual, Springer, 2008.

EC21308/EC22308: Mixed Signal RF IC Design

L	T	P/S	C
3	0	0	3

Total Hours: 42 Hrs.

Module 1 (9 hours)

CMOS comparators-Introduction to switched capacitor circuits - basic building blocks – operation and analysis –non ideal effects in switched capacitor circuits-switched capacitor integrators - First order filters –switch sharing –biquad filters.

Module 2 (10 hours)

Basic PLL topology, dynamics of simple PLL, Multiplier, EXOR and JK –flipflop phase detectors, lock acquisition, Phase frequency detector, Loop filters, Charge Pump PLLs, non ideal effects in PLLs.

Module 3 (13 hours)

Data converter fundamentals –DC and dynamic specifications –quantization noise – Nyquist rate D/A converters –decoder based converters –binary scaled converters – thermometer code converters –hybrid converters- Nyquist rate A/D converters-Successive approximation, Flash, interpolating, Folding, Pipelined, Time-interleaved converters

Module 4 (10 hours)

Oversampling converters, Noise shaping modulators, Decimating filters and interpolating filters, Higher **order** modulators, Delta Sigma modulators with multibit quantizers- Delta Sigma D/A

References:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, Tata-Mc GrawHill, 2002.
2. Rudy van de Plassche, CMOS integrated Analog- to Digital and Digital to- Analog converters, Kluwer academic publishers,2003.
3. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, 2001.
4. Roland E.Best, Phase Locked Loops, McGraw Hill,2007.
5. Richard Schreier, Understanding Delta-Sigma Data Converters, Wiley Interscience, 2005.
6. R.Jacob Baker, CMOS Mixed-signal Circuit Design, Wiley Student Edition, Wiley Interscience, 2009.

EC21309/EC22309: CMOS RF Circuit Design

L	T	P/S	C
3	0	0	3

Module 1 (12 hours)

Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers –Transmission lines Classical two-port noise theory, noise models for active and passive components, Noise figure, Friis equation, Nonlinearity and cascaded stages, Sensitivity and dynamic range, Passive impedance transformation.

Module 2 (12 hours)

High frequency amplifier design –zeros as bandwidth enhancers, shunt-series amplifier, fT doublers, neutralization and unilateralization Low noise amplifier design –LNA topologies, impedance matching, power constrained noise optimization, linearity and large signal performance, noise canceling LNAs, Constant gm biasing, current reusing technique.

Module 3 (10 hours)

Mixers –multiplier-based mixers, subsampling mixers, diode-ring mixers

RF power amplifiers –Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations.

Module 4 (8 hours)

Oscillators & synthesizers –describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.

References:

1. Thomas H. Lee, Cambridge, The Design of CMOS Radio-Frequency Integrated Circuits, UK: Cambridge University Press, 2004.

2. Behzad Razavi, RF Microelectronics, Prentice Hall, 1998.

3. A.A. Abidi, P.R. Gray, and R.G. Meyer, eds. Integrated Circuits for Wireless Communications, New York: IEEE Press, 1999.

4. Bosco Leung and Charles G. Sodini, VLSI for wireless communication, Second Impression, Pearson, 2009.

EC 21310/EC22310: III-V semiconductors and High Speed Electronic Devices

L	T	P/S	C
3	0	0	3

Module 1 (6 hours)

Wave Mechanics and the Schrödinger Equation, Free Particles, Bound Particles: Quantum Well, Charge and Current Densities, operators and current Densities, Expectation Value, Density of states. Electron and Phonons in Cryatals, Heterostructure, Quantum Well and Low dimensional system, Tunnelling Transport, Schrödinger Equation in Electric and Magnetic field, Scattering, 2DEG.

Module 2 (10 hours)

Important parameters governing the high speed performance of devices and circuits: Transit time of charge carriers, junction capacitances, ON-resistances and their dependence on the device geometry and size, carrier mobility, doping concentration and temperature; important parameters governing the high power performance of devices and circuits: Break down voltage, resistances, device geometries, doping concentration and temperature

Module3 (5 hours)

Materials properties:

Merits of III –V binary and ternary compound semiconductors (GaAs, InP, InGaAs, AlGaAs, SiC, GaN etc.), different SiC structures, silicon-germanium alloys and silicon carbide for high speed devices, as compared to silicon based devices,

Module 4 (8 hours)

Metal semiconductor contacts and Metal Insulator Semiconductor and MOS devices: Native oxides of Compound semiconductors for MOS devices and the interface state density related issues. Metal semiconductor contacts, Schottky barrier diode, Metal semiconductor Field Effect Transistors (MESFETs): Pinch off voltage and threshold voltage of MESFETs. D.C. characteristics and analysis of drain current. Velocity overshoot effects and the related advantages of GaAs, InP and GaN based devices for high speed operation. Sub threshold characteristics, short channel effects and the performance of scaled down devices.

Module5 (12 hours)

High Electron Mobility Transistors (HEMT): Hetero-junction devices. The generic Modulation Doped FET(MODFET) structure for high electron mobility realization. Principle of operation and the unique features of HEMT, InGaAs/InP HEMT structures: Hetero junction Bipolar transistors (HBTs): Principle of operation and the benefits of hetero junction BJT for high speed applications. GaAs and InP based HBT device structure and the surface passivation for stable high gain high frequency performance. SiGe HBTs and the concept of strained layer devices; High Frequency resonant – tunneling devices, Resonant-tunneling hot electron transistors.

Reference:

1. C.Y. Chang, F. Kai, GaAs High-Speed Devices: Physics, Technology and Circuit Applications Wiley
2. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons,
3. David K. Ferry, Ed., Gallium Arsenide Technology, Howard W. Sams & Co., 1985
4. Avishay Katz, Indium Phosphide and Related materials: Processing, Technology and Devices, Artech House, 1992.
5. S.M. Sze, High Speed Semiconductor Devices, Wiley (1990) ISBN 0-471-62307-5
6. Ralph E. Williams, Modern GaAs Processing Methods, Artech (1990), ISBN 0-89006-343-5,
7. Sandip Tiwari, Compound Semiconductor Device Physics, Academic Press (1991), ISBN 0-12-691740-X
8. G.A. Armstrong, C.K. Maiti, TCAD for Si, SiGe and GaAs Integrated Circuits, The Institution of Engineering and Technology, London, United Kingdom, 2007,ISBN 978-0-86341-743-6.
9. John H. Davies, " The Physics of Low-Dimensional Semiconductors an Introduction", Cambridge University Press, 1998.

EC21311/EC22311: VLSI for Signal Processing

L	T	P/S	C
3	0	0	3

Module 1(8 hours): Pipelining and Parallel Processing: introduction, pipelining of FIR Digital filters Parallel processing. Pipelining and parallel processing for low power.

Module 2(10 hours): Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques. Unfolding, Introduction An algorithms for unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding.

Module 3(8 hours): Folding: Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures Folding if Multirate systems.

Module 4(8 hours): Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.

Module 5(8 hours): Fast Convolution: Introduction, Cook, Toom algorithm, Winogard algorithm, iterated convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

References

1. Rafel C. Gonzalez and Richard E. Woods "Digital image processing", Addition-wisely
2. Anil K.Jain "Fundamental of digital image processing" prentice Hall 1995.
3. Rosenfeld A.C. Kak, Digital picture processing-academic press inc 1976.
4. Hall E.L. computer image processing and recognition academic press inc 1979.
5. Huang T.S. "Picture processing and digital filtering" Springer Verlag Berlin Heidelberg.